14.4 A 50mW HSDPA Baseband Receiver ASIC with Multimode Digital Front-End

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As data-centric applications proliferate in both cellular and local area networks, higher data rate expectations continue to precipitate new wireless standards, while popular incumbent standards must be retained in mobile terminals that have to shrink in size, improve power efficiency and lower cost. The amount of signal processing required for the latest 3G standards such as HSDPA poses stiff challenges to digital baseband processor designs in terms of both power consumption and chip size [1]. Such challenges are exacerbated by demands for multi-standard digital baseband solutions that should accommodate EDGE/WCDMA/HSDPA and, ideally, one or more non-cellular standards such as WLAN or WiMax. This case study aims to demonstrate that alternative partitioning of the baseband realization may allow power, size and reconfigurability to be better reconciled even with a cheaper technology.

Physical layer computations often require repetitive and costly operations such as multiply and correlate at high rates, as found in a UMTS modem. Both the RAKE receiver and turbo decoder for HSDPA translate to thousands of MIPS [2, 3] that are beyond any DSP today. Other functions such as matched filtering, equalization, symbol synchronization and carrier frequency tracking also require hundreds of MIPS that can benefit from a custom realization. If a RAKE accelerator ASIC should accompany the DSP core anyway and the protocol software resides in a microcontroller, an equally good case can be made for realizing the complete receiver in the ASIC without detriment to programmability. Such a receiver ASIC, optimized for low power and small area, is part of the present contribution.

In the quest for wireless modem reconfigurability, analog hardware is generally seen as an impediment and its reduction the focus for recent research. High performance A/D converters are an enabling component to this end and those based on ΔΣ modulation offer the best low-power solutions to date. The decimation filter required for such a converter is typically realized in ASIC form. Included in the baseband receiver IC to interface a multimode ΔΣ modulator reported separately [4], the decimation filter is combined with channel selection, RSSI and programmable gain control into a digital front-end (DFE) designed for multimode operation and optimized for power and area. Figure 14.4.1 shows the baseband receiver architecture that consists of a tri-mode ΔΣ modulator, a matching multimode DFE and a WCDMA/HSDPA receiver.

The DFE can be configured to decimate the modulator output for GSM/EDGE (26MHz), WCDMA/HSDPA (61.44MHz) or WLAN (220MHz) to 4 times their respective symbol rates. The 3 modes have totally distinct multiple access schemes and spread over two decades in signal bandwidth, which epitomizes the challenges to reconfigurability. The DFE architecture shown in Fig. 14.4.2 has been developed on the basis of overall considerations for reconfigurability, pulse shape, blocking template, adjacent channel selectivity and SNR needs in each mode, decimation ratio, speed, power, die area and latency. The combination of a cascade of 8 integrator-comb filters capable of decimating by up to 16, two half-band filters in transposed form each efficiently implementing decimation by 2, and a symmetric FIR filter with up to 63 taps and capable of decimating by up to 4, allows arbitrary decimation ratios up to 256 to be realized. Implementation details of the three filter types are shown in Fig. 14.4.3.

In the current application, the GSM/EDGE mode needs the most decimation (24), so that the CIC filter is programmed to decimate by 12, followed by one HBF. The UMTS mode requires decimation by 4, which is realized by only HBF filters for their power efficiency. In the WLAN mode the CIC filter is used to decimate by 5 and no HBF is used. In all three modes, the last FIR filter is used for matched filtering. In the UMTS mode, root-raised cosine matched filtering employs all 63 taps and its throughput must be 15.36MS/s. To ease the burden of 16 multiplications per clock cycle at 122.88MHz, 4 pipelined multiply-and-accumulate (MAC) units are used for both I and Q paths.

The main functions performed by a WCDMA/HSDPA receiver include symbol synchronization and spreading code generation, coarse and fine carrier frequency estimation and correction, RAKE receiver or an adaptive channel equalizer (for high rate HSDPA), and turbo decoder. The present implementation, shown in block diagram of Fig. 14.4.4, includes the RAKE receiver and all other necessary functions, but without the turbo decoder. Primary and secondary synchronization codes, scrambling group allocation table, as well as 15 possible OVSF channel codes are either precomputed and stored in a ROM, or calculated on the basis of those stored. A truncated version of the received signal is used for correlating with the PSCH and SSCH codes, which reduces the complexity of the symbol synchronization block without degrading the 1/4 chip accuracy. A lookup table is used to generate the sine wave used for rotating the received signals for fine tuning the carrier frequency. The 4-finger RAKE receiver is a challenging block, particularly in HSDPA mode, where up to 15 OVSF codes need to be correlated with the received signal within each chip period to decode aggregated user channels. Taking an area-conscious approach to this design, four high-speed adders have been used to perform complex-valued multiplications sufficiently fast to allow all 15 channel codes to be multiplexed to the given scrambling code and received data stream. When fewer multicodes are aggregated, clock signals are gated off during idle multiplex slots and corresponding unused registers shut down to save power.

Clock gating is aggressively used in this design, especially to take advantage of the multirate nature of the decimation filters and progressive data rate change within the WCDMA/HSDPA receiver due to despreading and variable code aggregation. The fact that blocks associated with symbol synchronization are used at different times to those of the other receiver blocks also enables parts to be shut down and gated off to save power. Altogether 226 gating blocks are distributed among both control and data paths that are divided into 23 clock domains, achieving a drastic reduction of dynamic power. To combat static power consumption due to leakage current, special care has been taken in timing optimization such that low V_t transistors are only used when necessary. The resulting static consumption is lower than 1mW.

Implemented in 0.13μm CMOS, the multimode DFE plus WCDMA/HSDPA receiver occupies 5mm^2. Figure 14.4.5 summarizes key features of the ASIC as well as measured results. Compared to the 0.5W-plus typical power consumption by commercial baseband solutions, the ASIC solution presented consumes 31mW in WCDMA mode and up to 48mW in HSDPA mode. A similar 10× advantage in die area makes the case for the ASIC compelling. Figure 14.4.6 shows measured BER performance of the chip with a spreading factor of 16 for WCDMA and HSDPA modes in a multipath environment.

Acknowledgments:
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References:
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[3] L. Gazsi, "Challenges in the Design and Diagnostics of Electronic Circuits and Systems and the Consequences," *DDECS Tutorial*, Apr., 2005.
[4] T. Christen, et al.,, "A 0.13μm CMOS EDGE/UMTS/WLAN Tri-Mode ΔΣ ADC with -92dB THD," *ISSCC Dig. Tech. Papers*, pp. 240-241, Feb., 2007.

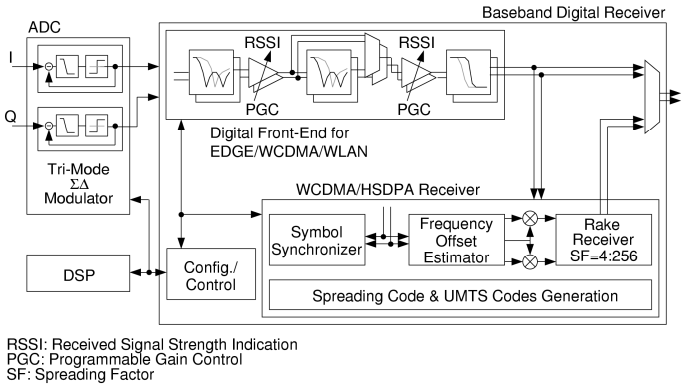

Figure 14.4.1: Baseband receiver architecture.

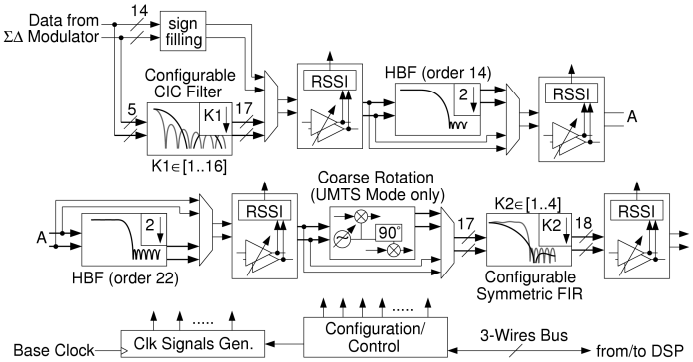

Figure 14.4.2: Digital front-end architecture.

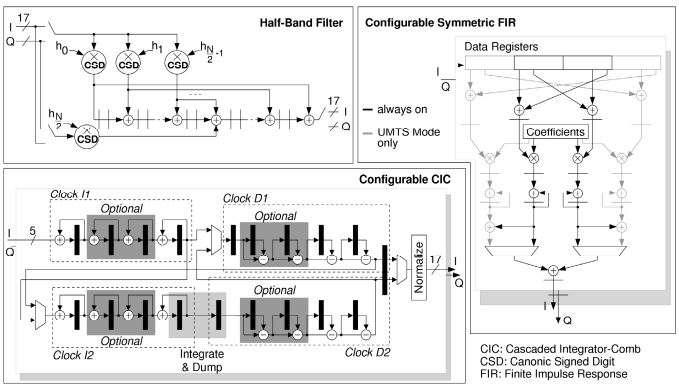

Figure 14.4.3: Architecture of the DFE filters.

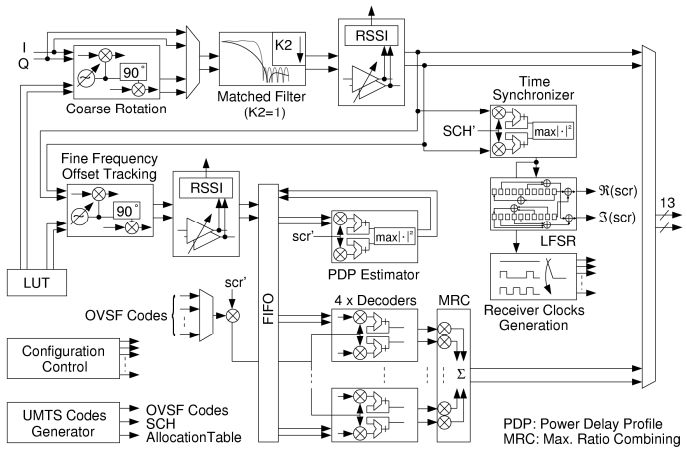

Figure 14.4.4: WCDMA/HSPDA receiver architecture.

	DFE Mode			
	GSM	**UMTS**	**WLAN**	**Unit**
Clock Frequency	26	122.88	220	MHz
Tot. Decimation Factor	24	4	5	
Out. Sample Rate	1.08	15.36	44	Ms/s
Signal BW (-3dB)	0.06	1.92	9	MHz
Peak SNR	99	76	75	dB
Power Consumption	0.8	18	31.2	mW
Core Supply	0.7	0.9	1.2	V

Base Clock Rate = 122.88MHz; Core Supply = 0.9V	**Power [mW]**
DFE + WCDMA Receiver (Output Data Rate = 60kbps)	31.1
DFE + WCDMA Receiver (Output Data Rate = 480kbps)	35.7
DFE + HSDPA Receiver (Output Data Rate = 7.2Mbps)	47.52
Core Leakage	0.66

Physical Characteristics		**Unit**
Technology	0.13µm 1P6M CMOS	
DFE Area	1.034	mm^2
Config. Block Area	0.07	mm^2
WCDMA Area	2.506	mm^2
Core Area	3.61	mm^2
Chip Area	5.15	mm^2

Figure 14.4.5: Key features.

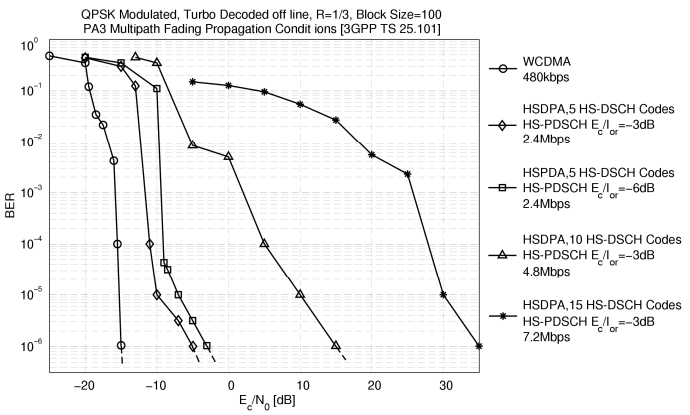

Figure 14.4.6: Measured BER (off-line turbo decoding).

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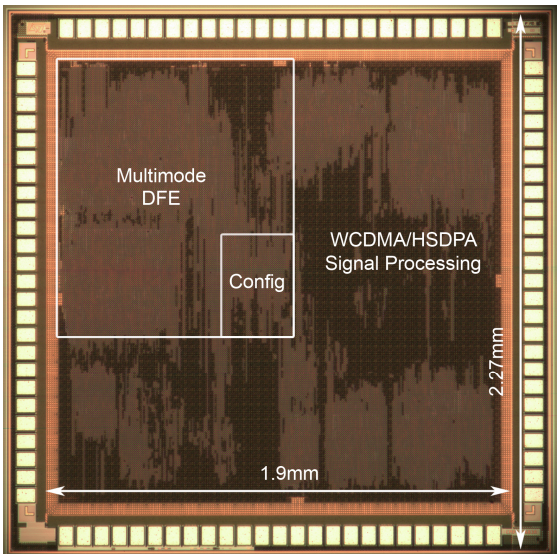

Figure 14.4.7: Die micrograph.

